WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

signal lines over which signals are transferred; and

a drive circuit driving the signal lines in operating modes,

the operating modes including a dynamic operation mode in which the signal lines are precharged, and a static operation mode in which the signal lines are not precharged.

2. The semiconductor device as claimed in claim 1, further comprising a memory cell array to which the signal lines are connected, data read from the memory cell array being transferred over the signal lines.

3. The semiconductor device as claimed in claim 1, further comprising a test-dedicated line,

a predetermined test of the semiconductor device being performed using the test-dedicated line and the signal lines.

4. The semiconductor device as claimed in

claim 3, further comprising a circuit receiving the signal lines at inputs thereof and outputting a test result, said test result and a logic level of the test-dedicated line forming a result of the predetermined test.

5. The semiconductor device as claimed in claim 3, further comprising a precharge circuit precharging the signal lines and the test-dedicated line.

6. The semiconductor device as claimed in claim 5, the precharge circuit precharging the signal lines and the test-dedicated line in the dynamic operation mode only.

7. A semiconductor device comprising:

signal lines over which signals are transferred; and

a circuit precharging the signal lines and then driving the signal lines on the basis of signals to be transferred in a first operation mode, and driving the signal lines on the basis of signals to be transferred in the absence of precharging in a second mode.

8. The semiconductor device as claimed in claim 7, further comprising a memory cell array to which the signal lines are connected, data read from the memory cell array being transferred over the signal lines.

9. The semiconductor device as claimed in claim 7, further comprising a test-dedicated line,

a predetermined test of the semiconductor device being performed using the test-dedicated line and the signal lines.

10. A semiconductor device comprising:

a signal line over which a signal is transferred;

first and second transistors respectively driving the signal line to a high level and a low level, respectively; and

a drive circuit controlling said first and second transistors to drive the signal line in first and second operating modes on the basis of a level of the signal to be transferred over the signal line, at least one of said first and second transistors further serving for precharging of the signal line,

the first operating mode needing precharging of the signal line and the second operating mode needing no precharging thereof.

11. A semiconductor device comprising:

signal lines over which signals are transferred;

first transistors respectively driving the signal lines to a high level;

second transistors respectively driving the signal lines to a low level; and

a circuit causing the second and first transistors to drive the signal lines precharged to the high and low levels in advance to the low and high levels in a first operating mode when the signals transferred are low and high, respectively, and causing the first and second transistors to the high and low levels on the basis of whether the signals transferred are high or low in a second operating mode.

12. The semiconductor device as claimed in claim 11, further comprising third transistors precharging the signal lines in the first operating mode in which the first and second transistors are OFF.

13. A semiconductor device comprising:

an internal circuit from which data items are supplied;

first signal lines over which signals corresponding to the data items are transferred;

a second signal line;

a drive circuit driving the first signal lines based on the data items and driving the second signal line based on the data items and a control

signal; and

a precharge circuit precharging the first and second signal lines in a given operating mode.

14. The semiconductor device as claimed in claim 13, further comprising a logic circuit making a given logical operation on the signals on the first signal lines.

15. The semiconductor device as claimed in claim 13, wherein the given operating mode is a test mode.

16. The semiconductor device as claimed in claim 13, wherein the internal circuit comprises a memory cell array.

17. A semiconductor device comprising:

an internal circuit from which data items are supplied;

first signal lines over which signals corresponding to the data items are transferred;

a second signal line;

a drive circuit driving the first signal lines based on the data items and driving the second

signal line based on the data items and a control signal; and

a precharge circuit precharging the second signal line in a given operating mode.

18. The semiconductor device as claimed in claim 17, wherein the drive circuit comprises transistors driving the first signal lines based on the data items, the transistors also precharging the first signal lines in the given operating mode.

19. The semiconductor device as claimed in claim 17, wherein the drive circuit comprises a logic circuit controlling the transistors on the basis of the data items and a control signal designating the given operating mode.

20. The semiconductor device as claimed in claim 17, wherein the internal circuit comprises a memory cell array.